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10/552,076	10/04/2005	Andrei Terechko	NL 030344	8796

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EXAMINER	
VICARY, KEITH E	
ART UNIT	PAPER NUMBER
2183	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,076	TERECHKO, ANDREI	
	Examiner	Art Unit	
	KEITH VICARY	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are pending in this office action and presented for examination.

Claims 1 and 5 are newly amended by amendment filed 1/11/2011.

Claim Objections

1. Claims 1-8 are objected to because of the following informalities. Appropriate correction is required.

a. In claim 1, line 6, "connections each" should be "connections, each".

i. Claims 2-4 are objected to for failing to alleviate the objection to claim 1 above.

b. In claim 5, line 6, "connections each" should be "connections, each".

c. In claim 5, line 7, "pipeline additional registers" should be "additional pipeline registers".

ii. Claims 6-8 are objected to for failing to alleviate the objection to claim 5 above.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Claim 1 recites the limitation “an instruction unit for issuing control signals to said clusters, wherein said instruction unit is connected to each of said clusters via respective control connections each control connection having a pipeline register" in lines 4-6. However, the instant disclosure does not support the concept of each control connection having a pipeline register. See, for example, any of Figures 1-4, which show no pipeline register between the instruction unit and clusters A and B. Consequently, each control connection does not have a pipeline register.

Applicant cites page 6, lines 25-30 and Figure 3 as providing support for the aforementioned limitation. However, Figure 3, as noted above, shows no pipeline register between the instruction unit and clusters A and B, and page 6, lines 25-30, likewise discloses that one or more pipeline registers are arranged in the control path CC and CD (but not CA or CB).

d. Claims 2-4 are rejected for failing to alleviate the rejection of claim 1 above.

5. Claim 5 recites the limitation “wherein said instruction unit is connected to each of said clusters via respective control connections each control connection having a pipeline register" in lines 5-6. However, the instant disclosure does not support the concept of each control connection having a pipeline register. See, for example, any of

Figures 1-4, which show no pipeline register between the instruction unit and clusters A and B. Consequently, each control connection does not have a pipeline register.

Applicant cites page 6, lines 25-30 and Figure 3 as providing support for the aforementioned limitation. However, Figure 3, as noted above, shows no pipeline register between the instruction unit and clusters A and B, and page 6, lines 25-30, likewise discloses that one or more pipeline registers are arranged in the control path CC and CD (but not CA or CB).

e. Claims 6-8 are rejected for failing to alleviate the rejection of claim 5 above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

8. Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108)

each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108).

However, Batten does not disclose each control connection having a pipeline register, and one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster.

On the other hand, Nickolls does disclose of control connections having a pipeline register, and one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

9. Consider claim 2, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

10. Consider claim 3, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

11. Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108) each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters

via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108).

However, Batten does not disclose each control connection having a pipeline register, and one or more pipeline additional registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster.

On the other hand, Nickolls does disclose of each control connection having a pipeline register, and one or more pipeline additional registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

12. Consider claim 6, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

13. Consider claim 7, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

14. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

15. Consider claim 4, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

16. Consider claim 8, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

Response to Arguments

17. Applicant states on page 5, first line, that claims 1 and 7 are independent. Examiner generally notes that claim 7 is dependent on independent claim 5.

18. Applicant argues on page 6 that the amendments in claims 1 and 5 are supported by the description. Specifically, applicant cites page 6, lines 25-30 and Figure 3 as providing support for the aforementioned limitation.

However, Figure 3, as noted above, shows no pipeline register between the instruction unit and clusters A and B, and page 6, lines 25-30, likewise discloses that one or more pipeline registers are arranged in the control path CC and CD (but not CA or CB).

Applicant further argues on page 6 the merit of the additional limitation "so as to pipeline said control connections to remote cluster among said clusters". Examiner generally notes that the additional limitation as argued is slightly different than that which is present in the amended claims. Regardless, this additional limitation does not alleviate the written description issue as explained in the previous paragraph and in the 112 section above.

19. Applicant argues on page 7 that applicant can find nothing in Batten or Nickolls, alone or in combination, that teaches particular amended limitations in claims 1 and 5, and consequently, it cannot render the present invention obvious.

However, applicant does not elaborate on this conclusion that the present invention is not obvious in view of Batten or Nickolls. Applicant does not address any facets of the rejection previously given which explained in detail how examiner believed Batten as modified by Nickolls taught portions of the independent claim limitations and which remain relevant to both previous and newly amended limitations. Consequently, examiner maintains the rejection.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH VICARY whose telephone number is (571)270-

1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Keith Vicary/
Examiner, Art Unit 2183

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183